CLAIM AMENDMENTS: DISCUSSION

Claim 68 has been amended to recite a method of forming a plurality of substantially evenly spaced pillars, the method comprising: forming a layer of a first material; depositing photoresist on the first material; patterning the photoresist using light having a wavelength of about 248 nm or more; etching the first material to form the plurality of substantially evenly spaced pillars, the pillars having a pitch between of about 220 nm. Support for this claim is found throughout the present applications, for example at paragraph [0061].

Claim 72 has been amended to recite the method of claim 68 wherein the pillars are portions of memory cells, and wherein the step of patterning the photoresist includes patterning photoresist pillars. Support for this claim amendment can be found, for example, at paragraphs [0060]-[0062].

Neither of these claim amendments constitutes new matter.

REMARKS

Section A summarizes the status of the claims. Sections B and C respond to the rejections of the Feb. 8 Office Action.

A. Status of the Claims

Claims 1-75 were pending in the application. Claim 75 has been cancelled. Claims 1-67 are withdrawn from consideration. Claims 68-71 were rejected under 35 USC 102(e) as being anticipated by Fritze et al., US Patent No. 6,934,007. Claims 68-75 were rejected under 35 USC 103(a) as being unpatentable over Fritze et al. in view of Lee et al., US Patent Publication No. 2002/0028541.

B. 35 USC 102(e) Rejections, Fritze et al.: Claims 68-71

Claims 68-71 were rejected under 35 USC 102(e) as being anticipated by Fritze et al.

Claim 68 has been amended to recite a method of forming a plurality of substantially evenly spaced pillars, the method comprising: forming a layer of a first material; depositing photoresist on the first material; patterning the photoresist using light having a wavelength of about 248 nm or more; etching the first material to form the plurality of substantially evenly spaced pillars, the pillars having a pitch between of about 220 nm.

The feature pitch of the photomask of Fritze et al. is about 250 nm (col. 3, line 28.) The Examiner will be aware that photolithographic technology is under constant pressure to reduce pitch and feature size, and thus that a reduction in pitch is a substantive achievement in this area and cannot be considered obvious.

Applicant has shown that claim 68, as amended, distinguishes over the cited reference, and respectfully requests withdrawal of the 35 USC 102(e) rejection of claims 68-71.

C. 35 USC 103(a) Rejections, Fritze et al. and Lee et al.: Claims 68-75

Claims 68-75 were rejected under 35 USC 103(a) as being unpatentable over Fritze et al. in view of Lee et al. Claim 75 has been cancelled.

Claim 68 has been amended to recite a method of forming a plurality of substantially evenly spaced pillars, the method comprising: forming a layer of a first material; depositing photoresist on the first material; patterning the photoresist using light having a wavelength of about 248 nm or more; etching the first material to form the plurality of substantially evenly spaced pillars, the pillars having a pitch between of about 220 nm.

In Section B of these Remarks, Applicant explained why this claim, as amended, distinguishes over the teachings of Fritze.

Claim 72 has been amended to recite the method of claim 68 wherein the pillars are portions of memory cells, and wherein the step of patterning the photoresist includes patterning photoresist pillars. In his rejection of claim 72, the Examiner finds that Fritze et al. does not teach that the pillars are portions of memory cells, but finds that Lee et al. teach memory cells including patterned pillars. The Examiner asserts:

> It would have been obvious to one having ordinary skill in the art to take the teachings of Fritze et al. and combine them with the teachings of Lee et al. in order to make the claimed invention because a photolithography method for closer pillar formation would be desired as the use of photolithography is the conventional way of producing features for a semiconductor device.

Recall that claim 72 recites that the step of patterning the photoresist includes patterning photoresist pillars. As described in paragraph [0141] of Lee et al. and Figs. 9a

and 9b, the pillars patterned by Lee et al. are formed in a two-step process: First Lee et al. depost a first photoresist layer, expose and develop the first photoresist layer to form first photoresist lines, then use the first photoresist lines to etch silicon lines. Next, Lee et al. deposit a second photoresist layer, expose and develop the second photoresist layer to form second photoresist lines orthogonal to the first photoresist lines, then use the second photoresist lines to etch silicon pillars. Photoresist is patterned into lines, but no photoresist *pillars* are formed.

The Examiner suggests that one skilled in the art would find it obvious to replace this two-step method of Lee et al. with the method of Fritze et al.

The two-step method of formation of Lee et al., however, is in fact necessary to the function of the memory cells. The method of Lee et al. produces square pillars, as the opposing sides of the square are each formed in one of the two steps. As Lee et al. describes (paragraph [0136]):

> For example, with a square or rectangular shaped pillar, a floating gate can be formed on each side of the silicon body or channel enabling four or more isolated floating gates to be formed around a single square pillar. In this way, multiple bits can be stored in each pillar memory.

The method of Fritze et al. described at col. 3, lines 20-29, in contrast, do not define opposing edges on the pillar, and will tend to produce rounded pillars, not the square pillars clearly preferred by Lee et al. Thus Lee et al. teaches against forming pillars using the method of Fritze et al.

The Examiner further quotes from paragraph [0399] of Lee et al.:

> For logic devices, in general, the size of the logic block is $(x+1)^2$ times the cell area, where (x) is the number of inputs on the logic gate. Since the cell area here can be as small as $4F^2$, where F is the minimum feature size (half-pitch), then for F=0.25 microns, the minimum area per logic gate is $4(F(x+1))^2$, or 2.25 microns squared for a 2-input NAND or NOR gate. Preferably, the area per logic gate is $4(F(x+1))^2$ to $5(F(x+1))^2$. This size includes an "isolation" row and column on each edge of the block, that is shared with the next block.

Applicant assumes the Examiner finds the feature size of .25 microns, or 250 nm, to be close to the size of Fritze et al. and to that of claim 68 and its dependent claims. Applicant respectfully points out, however, that this passage is speaking of feature size or *half-pitch*, not pitch. The pitch recited in the claim is 220 nm, where the half-pitch is 110 nm.

Applicant has shown that claims 68-75 are neither taught nor suggested by the Examiner's proposed combination of the teachings of Fritze et al. and Lee et al., and thus respectfully request reconsidcration.

CONCLUSION

In view of the preceding Remarks, Applicant submit that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicant **respectfully request an interview.** In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date

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